REMARKS

Claims 1-15 are pending in the application. Claims 1-15 have been rejected under 35 U.S.C. § 103(a) as being obvious over US Patent No. 6,413,872 (Takano). Claims 1, 6 and 11 have been amended. The legend for Figure 1 has been amended as suggested by the Examiner. No new matter has been added by these amendments. Support for the amendments may be found within the entirety of the specification, and particularly at pages 4-7.

I. Drawings

The objection to Figure 1 has been obviated by the attached replacement sheet.

II. 35 U.S.C. § 103

A. Independent claim 1

Independent claim 1 is directed to a method for designing a semiconductor interconnect architecture including a pair of metal layers interconnected by a plurality of conductive vias. The method includes determining via stress as a function of a via density. The method also includes positioning the plurality of conductive vias in the semiconductor interconnect architecture to provide a via density being at least as large as "a via density value below which the stress on a via does not significantly increase relative to the stress on the via above the via density value." Applicant respectfully submits that Kitch fails to disclose or suggest the limitations of independent claim 1.

Kitch relates to selected intersections of metal databases to create a database that defines a pattern of vias between lower and upper conductive layers. (Kitch, Abstract). The database of a pattern of vias allows interconnect vias to be optimized in size and shape to provide lowest possible interlayer resistance. In Kitch, the allowable via size between upper and lower metal structures is determined for existing metal interconnect structures. Kitch illustrates a method for forming a self-aligned aluminum pillar for use as a conductive via post to connect upper and lower conductive interconnect layers in a semiconductor device. (Kitch, col. 4, ll. 19-23). Kitch applies to the formation of individual via interconnects at an intersection of upper and lower mask databases. (Kitch, col. 4, ll. 1-16). Indeed, Kitch illustrates the principles with respect to the formation of an individual via. (Kitch, Figs. 6-11c; col. 4, ll. 19-23). Accordingly, Kitch applies to optimizing the size and shape of an individual via without respect to other vias in an interconnect architecture and without respect to via density.

Applicant submits that Kitch does not disclose or suggest the limitations of claim 1. First, Kitch fails to disclose determining via density, as recited in claim 1. In particular, Kitch does not disclose determining via stress as a function of a via density, where via density includes "a ratio of the plurality of conductive vias interconnecting the pair of metal layers to an area of the pair of metal layers." Next, Kitch does not disclose positioning the plurality of conductive vias in the semiconductor interconnect architecture according to a via density, as recited by claim 1. Figure 12 illustrates a plurality of vias resulting from the via pillar formation process disclosed by Kitch. (Kitch, Fig 12, col. 6, ll. 64-67). However, Kitch fails to disclose relative positioning of the vias in the interconnect architecture and also fails to disclose positioning according to a via density determination. Accordingly, Applicant submits that Kitch does not disclose or suggest the limitations of claim 1, and therefore, claim 1 would not be obvious to one skilled in the art in light of Kitch. Applicant respectfully requests reconsideration of the rejection of claim 1.

B. Independent claim 6

Independent claim 6 is directed to a method of producing a semiconductor interconnect architecture. The method includes "determining via stress as a function of a via density." The via density is a ratio of a plurality of conductive vias interconnecting a first and second metal layer and an area occupied by the metal layers. The conductive vias are positioned in the semiconductor interconnect architecture according to a via-to-metal area ratio. The via-to-metal area ratio is at least as large as a predetermined via-to-metal area ratio value below which the stress on the vias does not significantly increase relative to the stress on the vias above the value.

Applicant submits that Kitch does not disclose or suggest the limitations of independent claim 6. As discussed, Kitch relates to the forming individual via interconnects at an intersection of upper and lower mask databases to optimizing the size and shape of an individual via without respect to other vias in an interconnect architecture and without respect to via density. However, Kitch does not disclose or suggest "determining via stress as a function of a via density," as recited by claim 6. Moreover, Kitch fails to disclose positioning the plurality of conductive vias in the semiconductor interconnect architecture according to a via-to-metal area ratio being at least as large as a predetermined via-to-metal area ratio value below which the stress on the vias does not significantly increase relative to the stress on the vias above the value," as recited by claim 6. Indeed, nothing in Kitch discloses or suggests the relative position of vias or positioning of vias in accordance with via density. Accordingly, Applicant respectfully submits that claim 6 would not have been obvious to one skilled in the art. Applicant requests reconsideration of claim 6.

B. Independent claim 11

Independent claim 11 is directed to a semiconductor interconnect architecture. The interconnect architecture includes a plurality of conductive vias "arranged with respect to the first metal layer and the second metal layer according to a via-to-metal area ratio being at least as large as a predetermined via-to-metal area ratio value below which stress on the plurality of vias does not significantly increase relative to stress on the vias above the value." As discussed, Kitch relates to the forming individual via interconnects at an intersection of upper and lower mask databases to optimizing the size and shape of an individual via without respect to other vias in an interconnect architecture and without respect to via density. Nothing in Kitch discloses or suggests an arrangement of a plurality of vias according to via-to-metal ratio. Indeed, nothing in Kitch discloses or suggests arranging the vias according to "via-to-metal area ratio being at least as large as a predetermined via-to-metal area ratio value below which stress on the plurality of vias does not significantly increase relative to stress on the vias above the value." Accordingly, claim 11 would not have been obvious to one skilled in the art in view of Kitch. Applicant respectfully requests reconsideration of the rejection of claim 11.

Dependent Claims

For similar reasons, Kitch also fails to disclose the limitations of claims 2-5, 7-10 and 12-15. As discussed above, Kitch does not disclose or suggest the limitations for independent claims 1, 6 and 11, and therefore, Kitch also does not disclose the limitations for claims dependent therefrom. Accordingly, Applicants also respectfully request favorable consideration of claims 2-5, 7-10 and 12-15.

CONCLUSION

In view of the foregoing amendments and reasons, Applicant respectfully requests favorable consideration and earnestly solicits allowance of all pending claims. Inquiries regarding this communication may be directed to the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes the designation of the legend "Prior Art" for Fig. 1, as suggested by the Examiner. Withdrawal of the pending objection to Figure 1 is respectfully requested.

Attachment: Replacement Sheet